SGS-THOMSON MICROELECTRONICS

STV1601A

SERIAL INTERFACE TRANSMISSION ENCODER

THIS IC CONTAINS ALL THE CIRCUITS NEEDED FOR CONVERSION FROM PARALLEL DATA, AND PARALLEL CLOCK, INTO SERIAL DATA. APPLICATIONS ARE STRAIGHTFORWARD AS ONLY A FEW EXTERNAL COMPONENTS ARE NEEDED.

OTHER RELATED IC's INCLUDE :

- STV1602A, A SERIAL TRANSMISSION DECODER (WITH A BUILT-IN CABLE EQUALIZER AND PARALLEL-TO-SERIAL CONVERSION)
- STV1389AQ COAXIAL CABLE DRIVER

STRUCTURE

- Hybrid IC

APPLICATIONS

SERIAL DATA TRANSMISSION ENCODER

- 100 to 270 Mb/s

APPLICATIONS EXAMPLES

- Serial data transmission of digital television signal 525-625 lines
- 4:2:2 component 270Mb/s (10-BIT)
- 4*FSC PAL composite 177Mb/s (10-BIT)
- 4*FSC NTSC composite 143Mb/s (10-BIT)

FUNCTIONS

- Parallel-to-serial conversion
- Scrambler : Modulo - 2 division by $G(x) = (x^9 + x^4 + 1)(x + 1)$
- PLL for serial clock generation
- PLL lock detection
- Sync word required with the parallel data stream

	8 bit	10 bit
1st word	FFH	3FFH
2nd word	00H	000H
3rd word	00H	000H

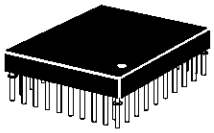
Sync word conversion (8-bit timing reference signal is internally converted to 10-bit).

CODE LIMITATION

The word composing the Sync word listed above shall not appear during data words.
This limitation includes 00 and FF in 8-bit use and 000 through 003 and 3FC through 3FF in 10-bit use.

DESCRIPTION

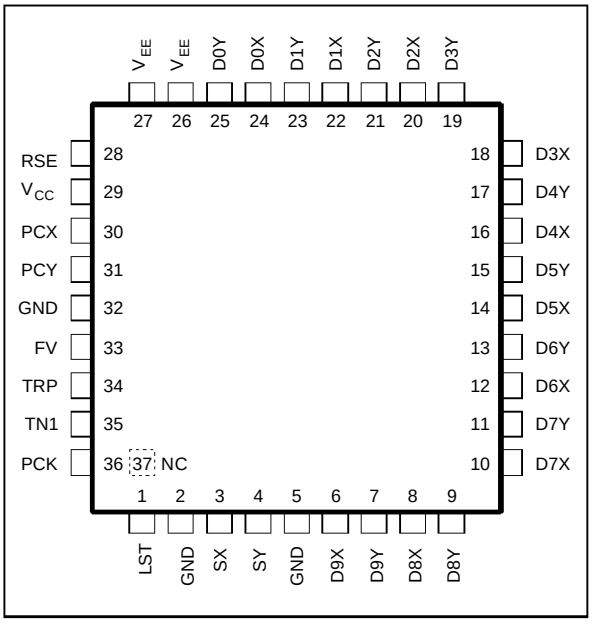
The STV1601A is a Hybrid IC encoder that converts parallel data into serial data for a serial transmission line.



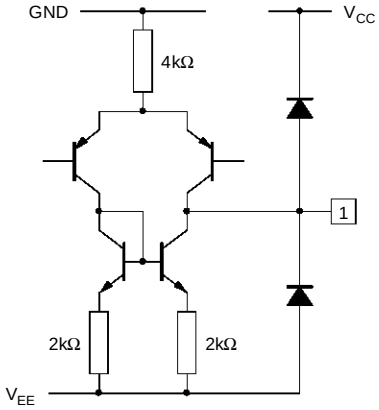
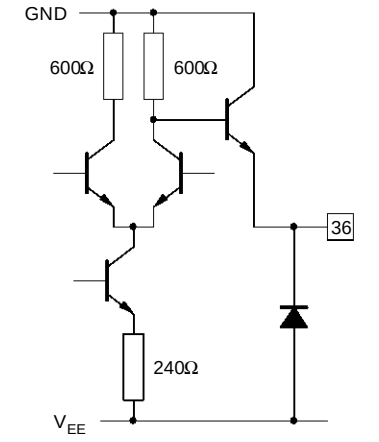
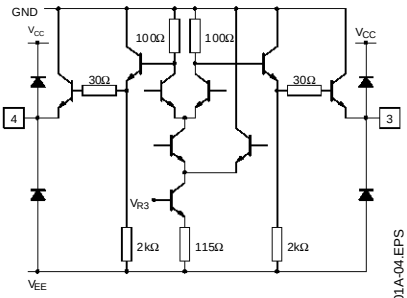
PGA37
(Ceramic Package)

ORDER CODE : STV1601A

PIN CONNECTIONS



PIN DESCRIPTION

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
1	LST		PLL lock detection. Is High while PLL locked. If unlocked, becomes irregular. At free running (TN1 H) turns Low H L	O	 -1.0		 -4.0	 V V
36	PCK		Clock output frequency divided to 1/10 VCO output. Used to check VCO free running frequency H L	O		 -0.8 -1.6		 V V
3	SX		Differential Serial Output Input parallel data is converted to serial, then from scrambled NRZ to NRZI data H L	O		 -1.6 -2.4		 V V
4	SY							

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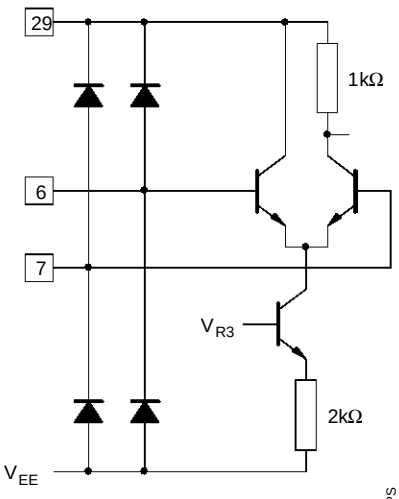
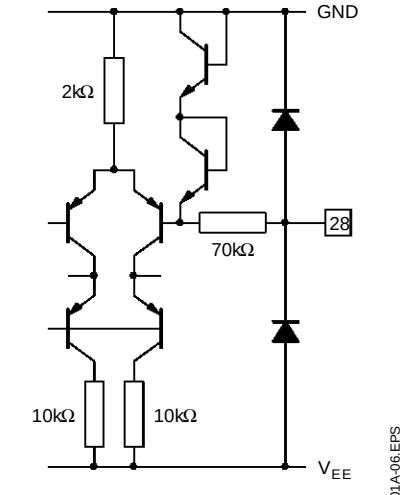
PIN DESCRIPTION (continued)

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
29	V_{CC}		Parallel data and clock input buffers power supply. When this pin is connected to +5V, parallel data clock turns to TTL mode. When this pin is connected to GND, parallel data clock turns to ECL mode.	-				
6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	D9X D9Y D8X D8Y D7X D7Y D6X D6Y D5X D5Y D4X D4Y D3X D3Y D2X D2Y D1X D1Y D0X D0Y		Parallel input ports: LSB : D0X or Y MSB : D9X or Y Signal : DnX Return : DnY For ECL mode, V_{CC} shalll be 0V H L ForTTL mode, VCC shall be +5V H L		 -1.0 2.0	 -1.6 0.8	 V V V V
28	RSE		VCO range selection H : high range 140 to 270MHz L : low range 100 to 145MHz H L	I	 -0.4		 -4.0	 V V

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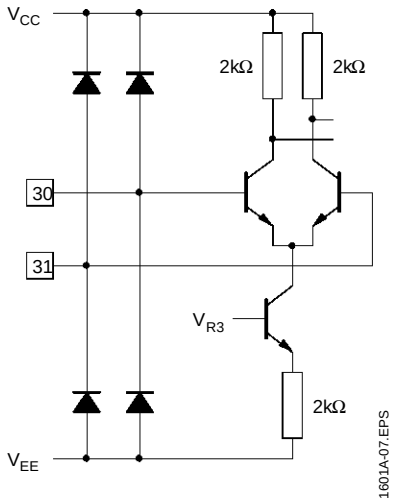
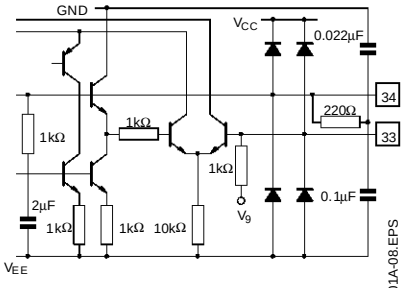
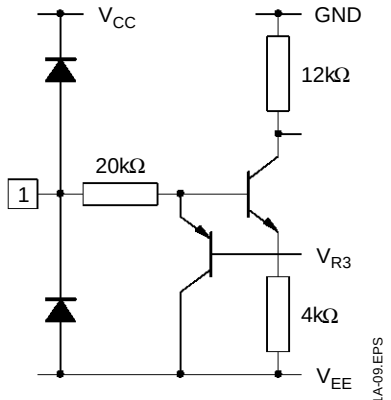
PIN DESCRIPTION (continued)

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
30	PCX		Parallel clock (PCX) and its return (PCY) For ECL mode, V_{CC} = 0 H L For TTL mode, V_{CC} = +5V H L	I	 -1.0 2.0		 -1.6 0.8	 V V V V
31	PCY							
2, 5, 32	GND		GND					
26	V_{EE}		-5V power supply I/O buffer PLL		-5.2	-5.0	-4.8	V
27	V_{EE}		-5V power supply Logic part		-5.2	-5.0	-4.8	V
33	FV		VCO free running frequency adjustment : V_{EE} level gives the lowest frequency. To adjust, set TN1 high.	I		-3.9		V
34	TRP		VCO input and phase comparator output should be connected to a parallel clock frequency trap filter to minimize jitter	O		-3.2		V
35	TN1		Test mode : High : VCO free running condition (input disabled) Low : Normal mode (input enabled)	I	-1.0		 -4.5	V V

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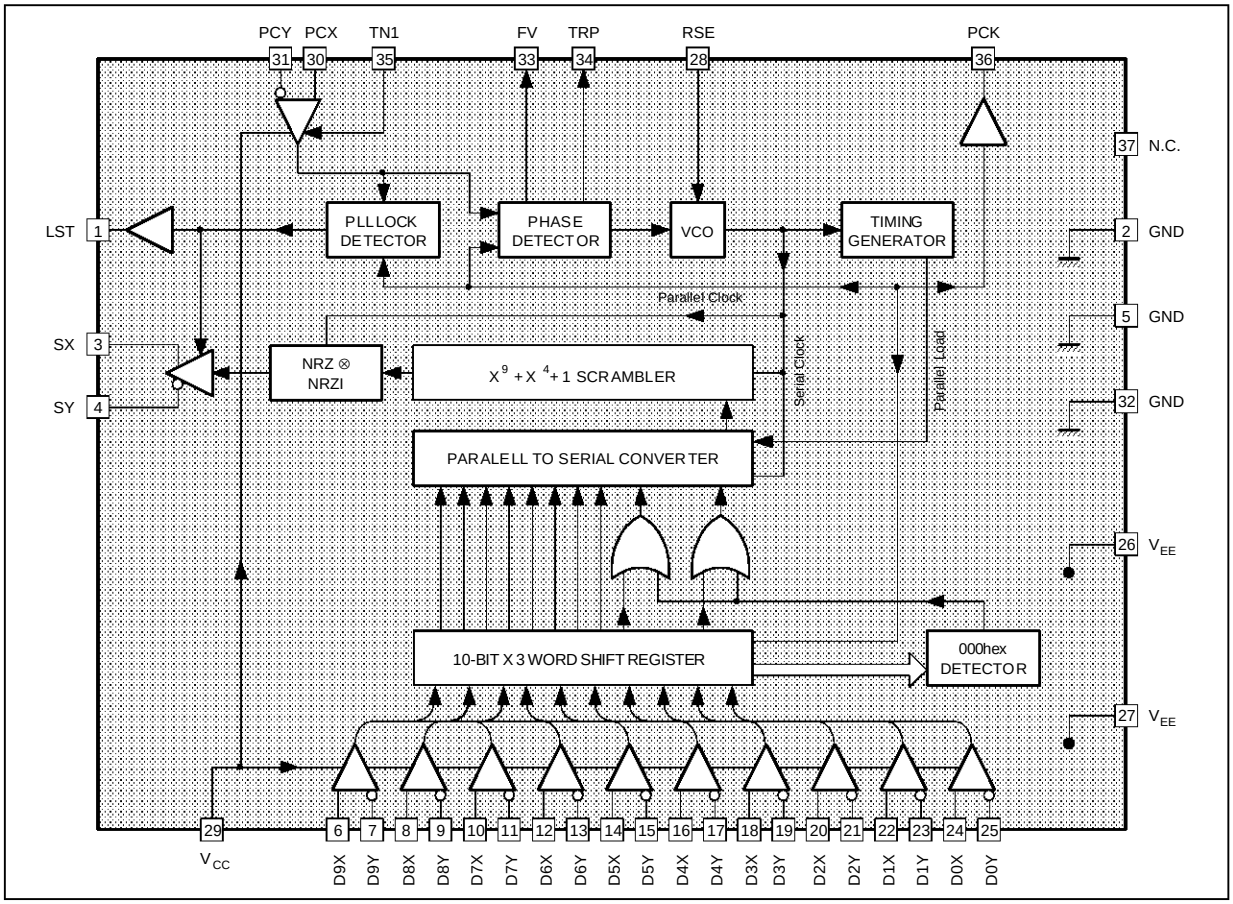
BLOCK DIAGRAM



1601A-10.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-6	V
V_{CC}	Supply Voltage	+6	V
V_{IN}	Input Voltage	V_{EE} to V_{CC}	V
I_{OUT}	Output Current	-30	mA
T_{oper}	Operating Temperature	0 to 65	°C
T_{stg}	Storage Temperature	-50 to 125	°C
P_D	Allowable Power Dissipation	2.0	W

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-4.8 to -5.2	V
V_{CC}	Supply Voltage *	4.8 to 5.2	V
T_{oper}	Operating Temperature	0 to 65	°C

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* For TTL input. Voltages are given with respect to GND

ELECTRICAL CHARACTERISTICS (V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise speciied)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{EE}	Supply Current 1		Figure 2		140		mA
I_{CC}	Supply Current 2				7		mA

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ELECTRICAL CHARACTERISTICS (V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise speciied)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
V_{IH}	Input Voltage	V_{CC} = GND PCX, PCY, DnX, DnY		-1.0			V
V_{IL}						-1.6	V
V_{IH}		V_{CC} = +5V PCX, PCY, DnX, DnY		2.0			V
V_{IL}						0.8	V
I_{IH}	Input Current	PCX, PCY, DnX, DnY	Figure 3			5	µA
I_{IL}				-1		+1	µA
V_{IH}	Input Voltage	RSE	Figure 7	-0.4			V
V_{IL}						-4.0	V
V_{IH}		TN1	Figure 6	-1			V
V_{IL}						-4.5	V
V_{OH}	Output Voltage	PCK R_P = 1kΩ			-0.8		V
V_{OL}					-1.6		V
V_{OH}		LST I_{OH} = -10µA, I_{OL} = +10µA	Figure 5	-1.0			V
V_{OL}						-4.0	V
V_{OH}		SX, SY R_P = 220Ω			-1.6		V
V_{OL}					-2.4		V
AC CHARACTERISTICS							
f_{MAX1}	VCO Max. Oscillation Frequency 1	RSE = "H"	Figure 4	30.0			MHz
f_{MIN1}	VCO Min. Oscillation Frequency 1					14.0	MHz
f_{MAX2}	VCO Max. Oscillation Frequency 2	RSE = "L"		15.0			MHz
f_{MIN2}	VCO Min. Oscillation Frequency 2					10.0	MHz
f_{HP1}	PLL Pull in Range	f signal = 270MHz RSE = "H"	Figure 1	27.7			MHz
f_{LP1}						25.5	MHz
f_{HP2}		f signal = 177MHz RSE = "H"		18.8			MHz
f_{LP2}						16.5	MHz
f_{HP3}		f signal = 143MHz RSE = "H"		15.0			MHz
f_{LP3}						13.0	MHz
f_{OP1}	PLL Generator Frequency	RSE = "H"		14.0		27.0	MHz
f_{OP2}		RSE = "L"		10.0		14.5	MHz
tjit	Jitter	f signal = 270MHz RSE = "H"	Figure 8			±0.25	nsec

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Tested through PCK : 1/10 of serial clock.

SWITCHING CHARACTERISTICS (V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise speciied)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_r	Rise Time	PCK R_P = 1kΩ	Figure 10		0.8		nsec
t_f	Fall Time				1.4		nsec
t_r	Rise Time	SX, SY R_P = 220Ω			0.7		nsec
t_f	Fall Time				0.7		nsec

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TIMING RELATION OF INPUT CLOCK AND DATA

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_w	Pulse Width	PCX, PCY	Figure11	-5 + t_c/2	t_c/2	+5 + t_c/2	nsec
t_d	Delay Time	PCX - Dn		-5		+5	nsec

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Figure 1 : Test Circuit Diagram Example

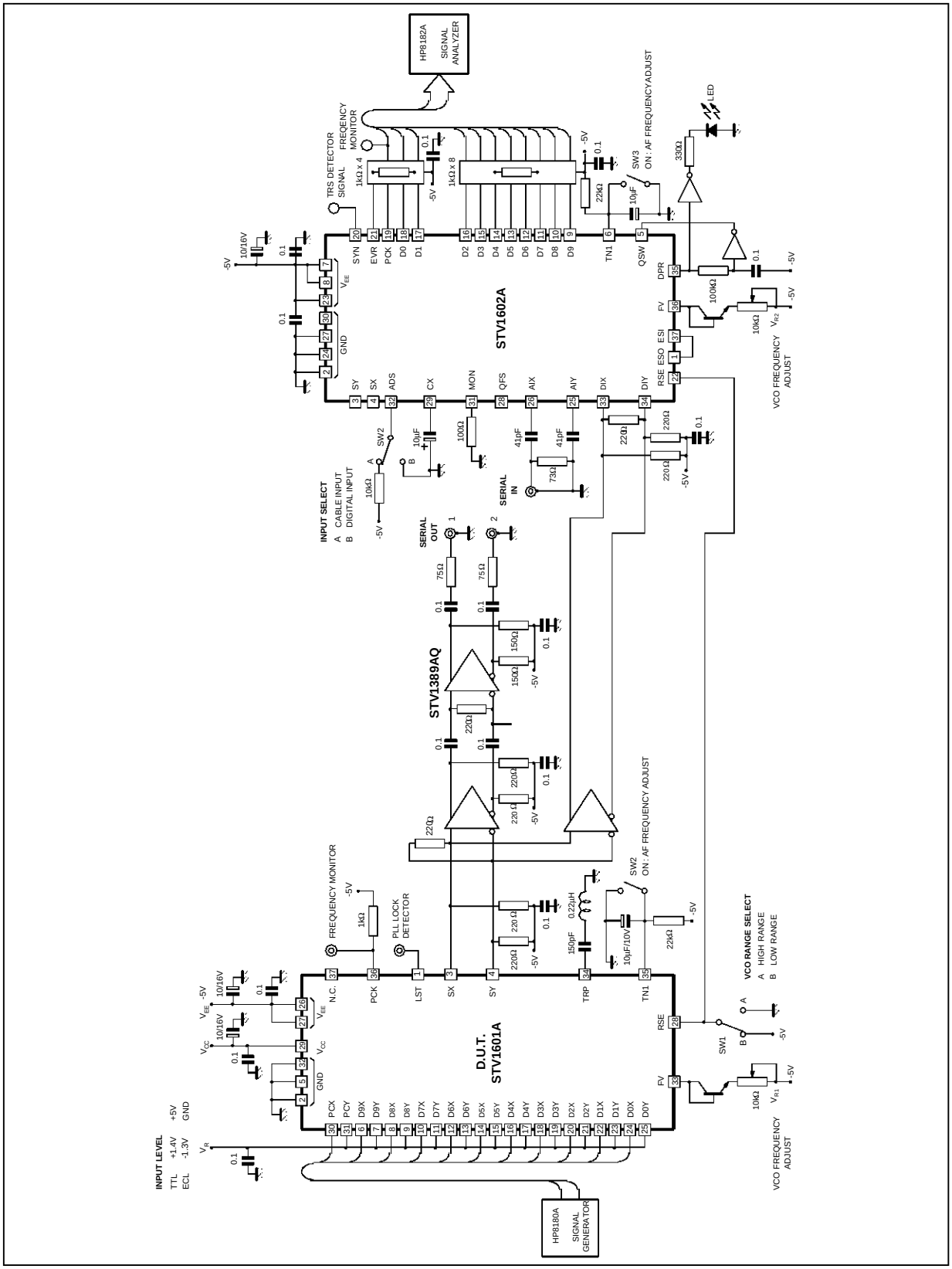


Figure 2

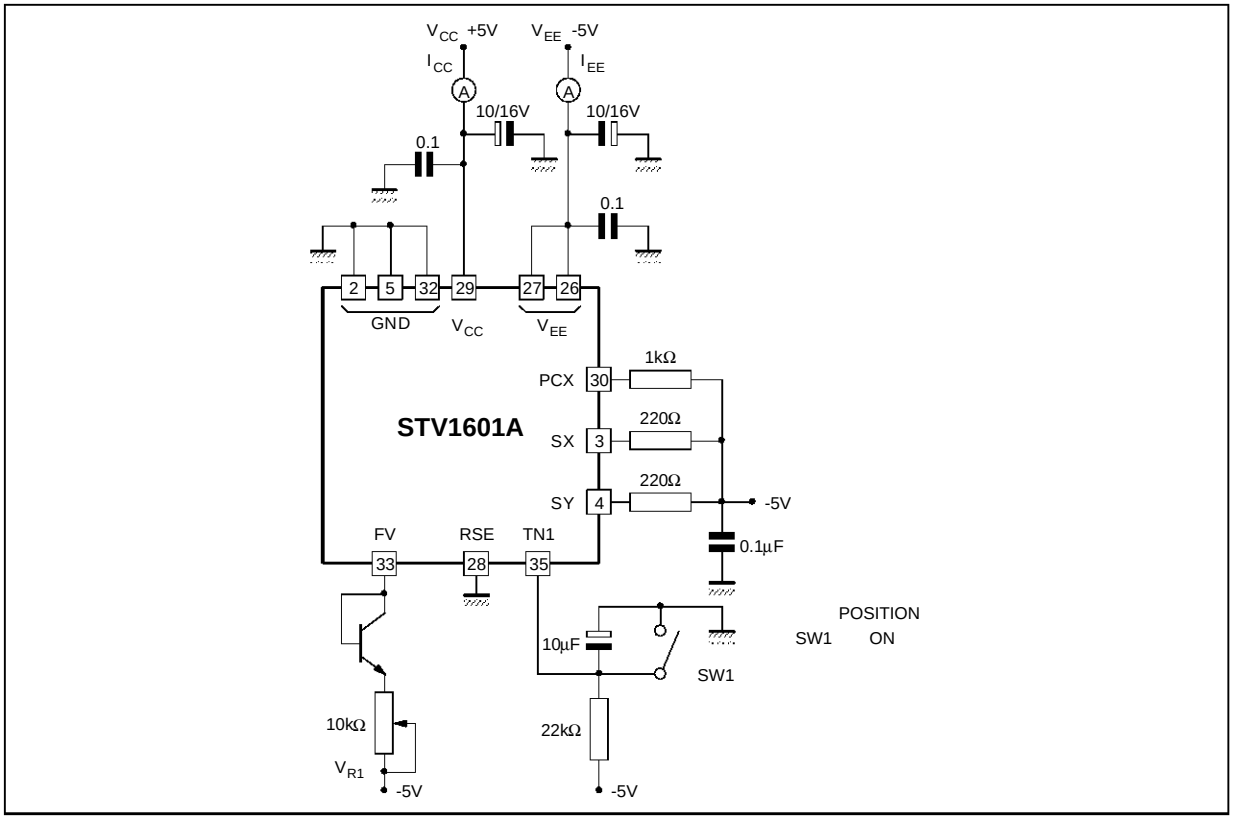


Figure 4

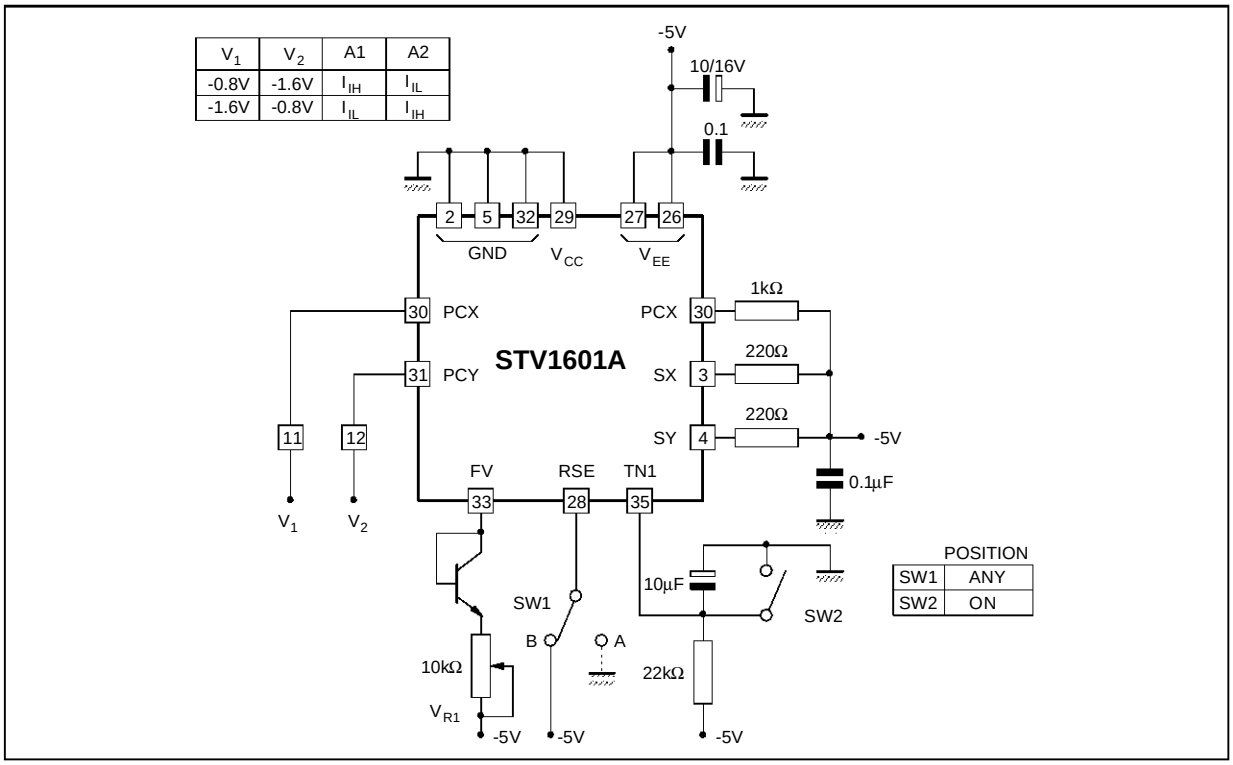


Figure 4

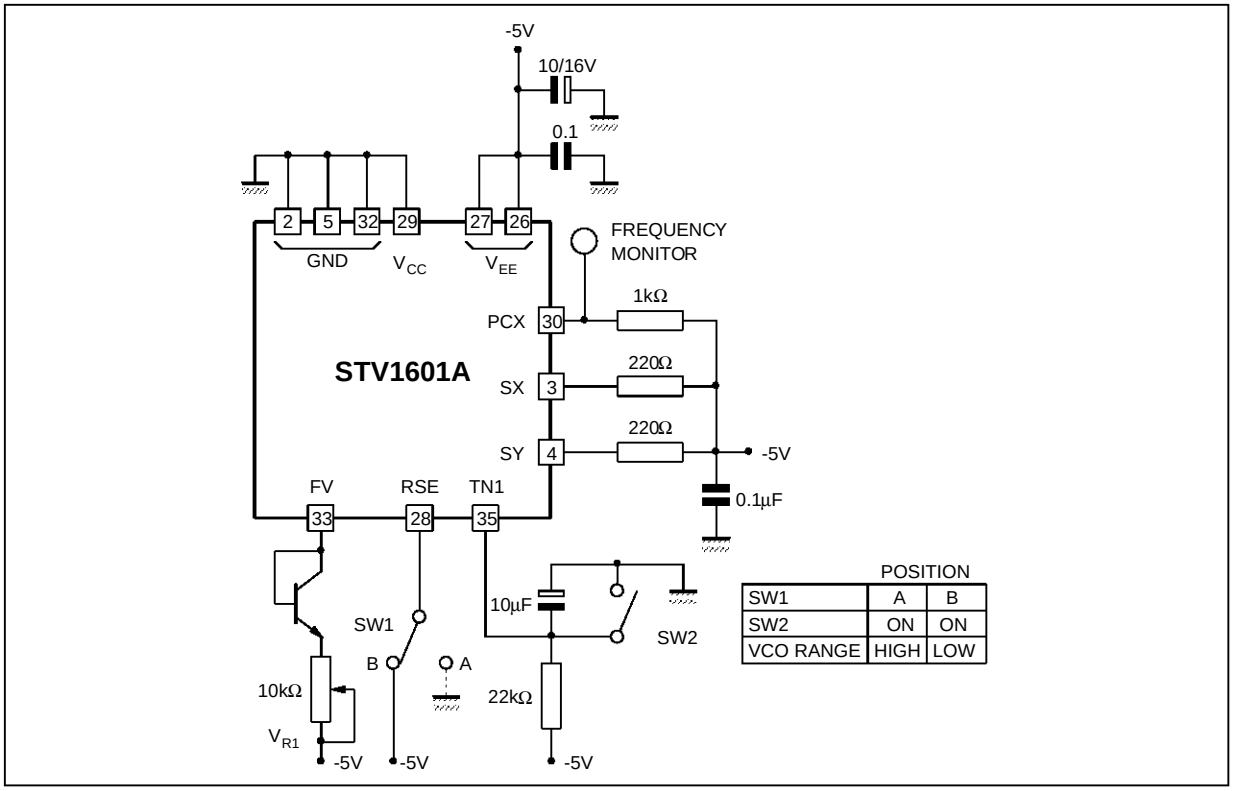


Figure 5

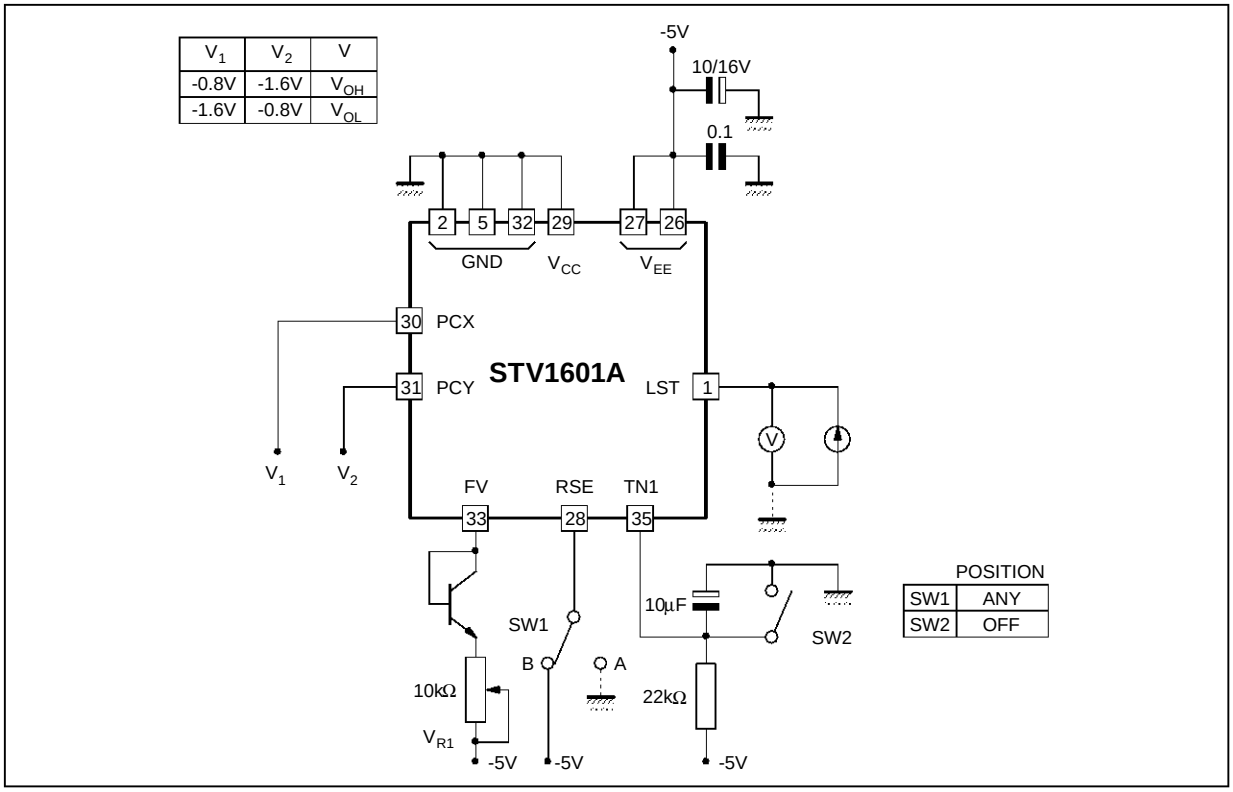


Figure 6

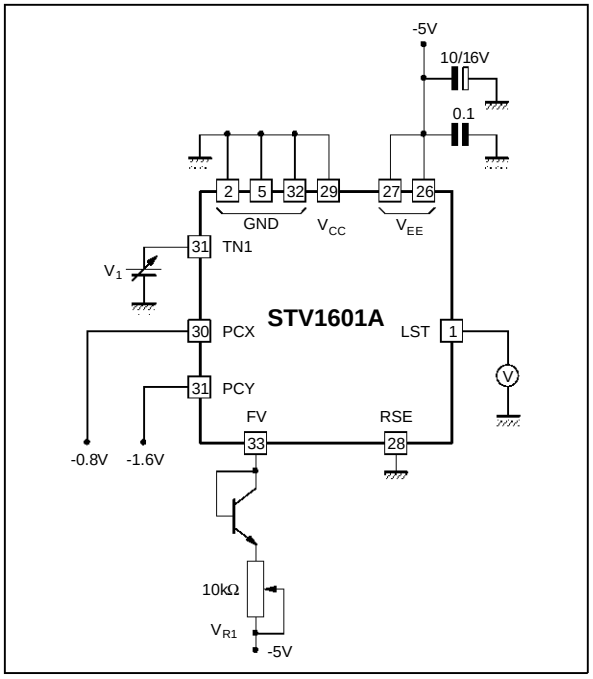


Figure 7

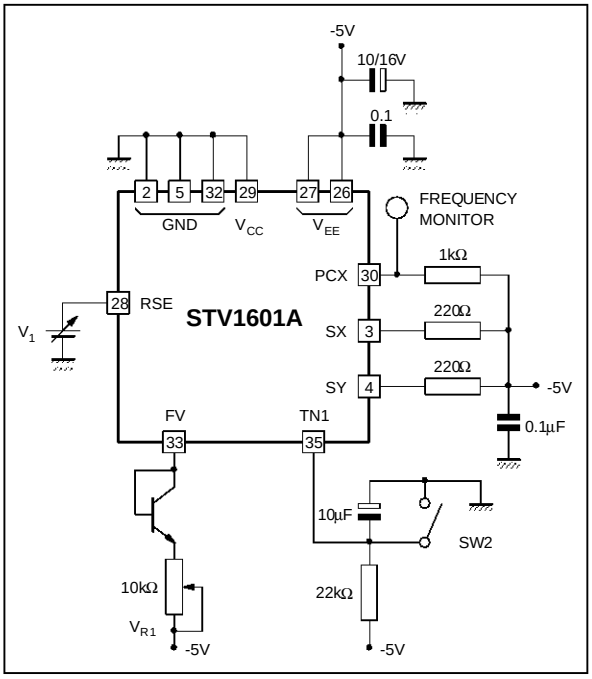


Figure 8

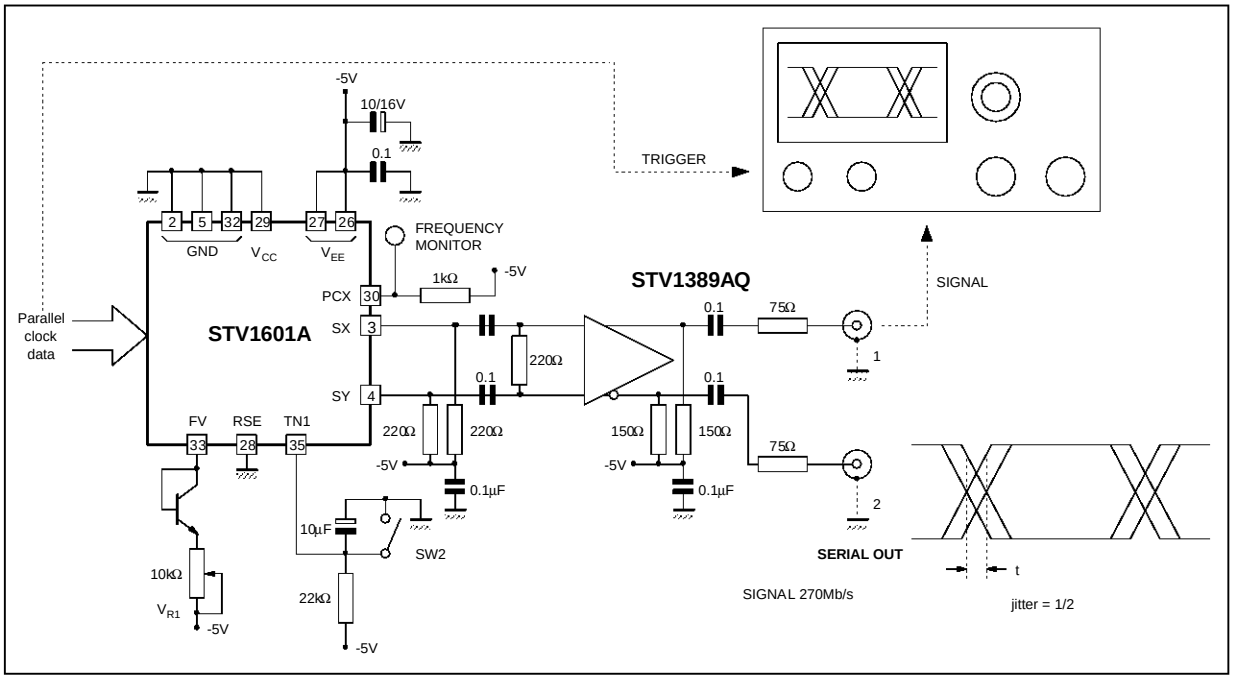


Figure 9 : t_r, t_f Definition

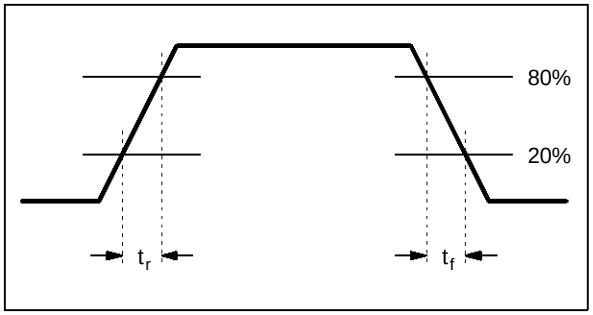
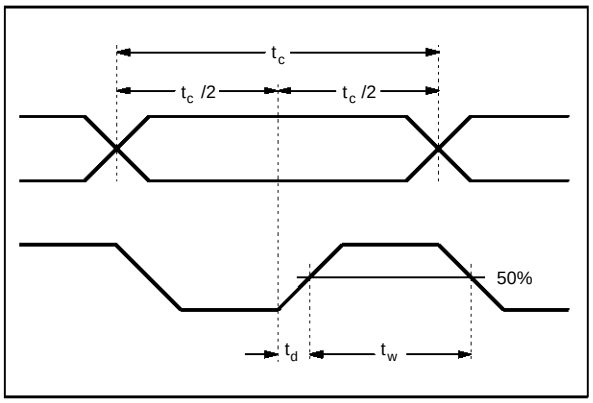


Figure 10 : t_d, t_W Definition



DESCRIPTION

STV1601A internally generates a 10 times clock frequency locked to the parallel input clock thanks to a built-in PLL and converts input parallel data into serial data.

To ease clock extraction at the receiving end, serial data is scrambled. To minimize polarity effect, serial data is then converted to NRZI and output in differential mode.

A PLL lock detection circuit only enables the serial output when locked.

1. Phase relation between input parallel clock and data

The phase relation between the parallel clock and the data is shown in Figure 11. Both clock and data are differential inputs

Parallel clock and data are such that the rising edge of PCX should be at the middle of the data. A clock having the same phase as PCX is internally generated in order to latch the data.

2. TTL input operation

Parallel clock and data can be either TTL or ECL inputs. To use as TTL inputs VCC (Pin 29) shall be connected to +5V. A fixed bias of +1.4V shall be applied to PCY and DnY (n = 0 to 9). TTL signals and their parallel clock will be provided through 1kW resistors to each "X" input. These 1kW resistors are effective to minimize the influence of the TTL input signals to the jitter characteristics of the serial output signal. For 8-bit data, unused LSB(s) must be fixed Low. Fixed bias value can be higher, for example, 2.5V in case of CMOS inputs.

Figure 11 : Phase Relation between Clock and Data

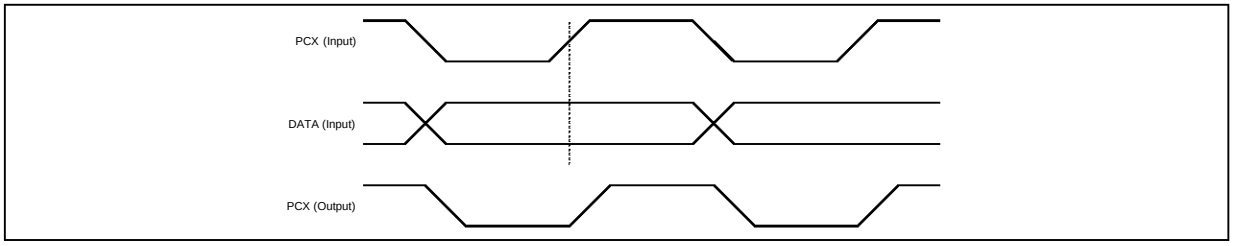
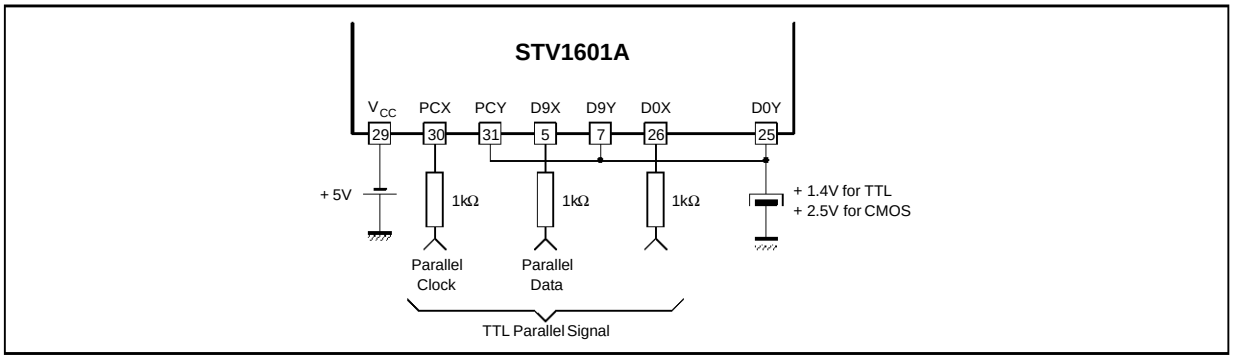


Figure 12 : TTL Input Operation



3. PLL block

PARALLEL CLOCK INPUT CONTROL

PLL, PLL lock detection and the various blocks of the serial output control are shown in Figure 13. When TN1 is connected to GND (set High), the parallel clock input is disabled.

The VCO turns to free running conditions and its frequency can be adjusted through FV.

This frequency decreases when the resistor value between FV and V_{EE} is reduced. Oscillation frequency monotoring is performed through PCK which delivers a frequency divided by ten.

When PLL is locked, PLL and PCX input signal phases are nearly matched. The RC network connected to TN1, temporarily, disables the parallel clock in order to avoid mislocking problems.

VCO oscillation frequency range selection is available through RSE ; High : from 140 to 270MHz ; Low : from 100 to 145MHz.

TRP (Pin 34) is the phase comparator output. To minimize jitter, a trap circuit, consisting in a serial tuned circuit at parallel clock frequency can be used.

PLL LOCK DETECTION

The LST signal is generated by latching the incoming parallel clock by the internal one (which is 1/10 of the VCO frequency). LST is used as a PLL lock detection signal and also controls the serial output.

If the parallel clock input is disabled (by means of TN1), LST turns Low and the serial output is disabled as described in the previous section (SX (Pin 3) = High, SY (Pin 4) = Low).

If the serial output has to be disabled while no parallel clock input is provided, PCX must be set Low and PCY must be set High.

4. Sync word

To convert serial data back to parallel, insertion of some timing reference data indicating the parallel data word boundary in the serial data is needed. This, called TRS (Timing Reference Signal) in the digital interface format, consists of the three consecutive words 3FFH, 000H, 000H.

Conversion to 10-bit TRS from 8-bit (TRS)

8-bit parallel data

8-bit parallel data can be converted into 10-bit data by using the 8th bit as the MSB and by setting the 2 LSBs at logical states as shown in Figure 14.

Figure 13 : PLL and Serial Output Control Block

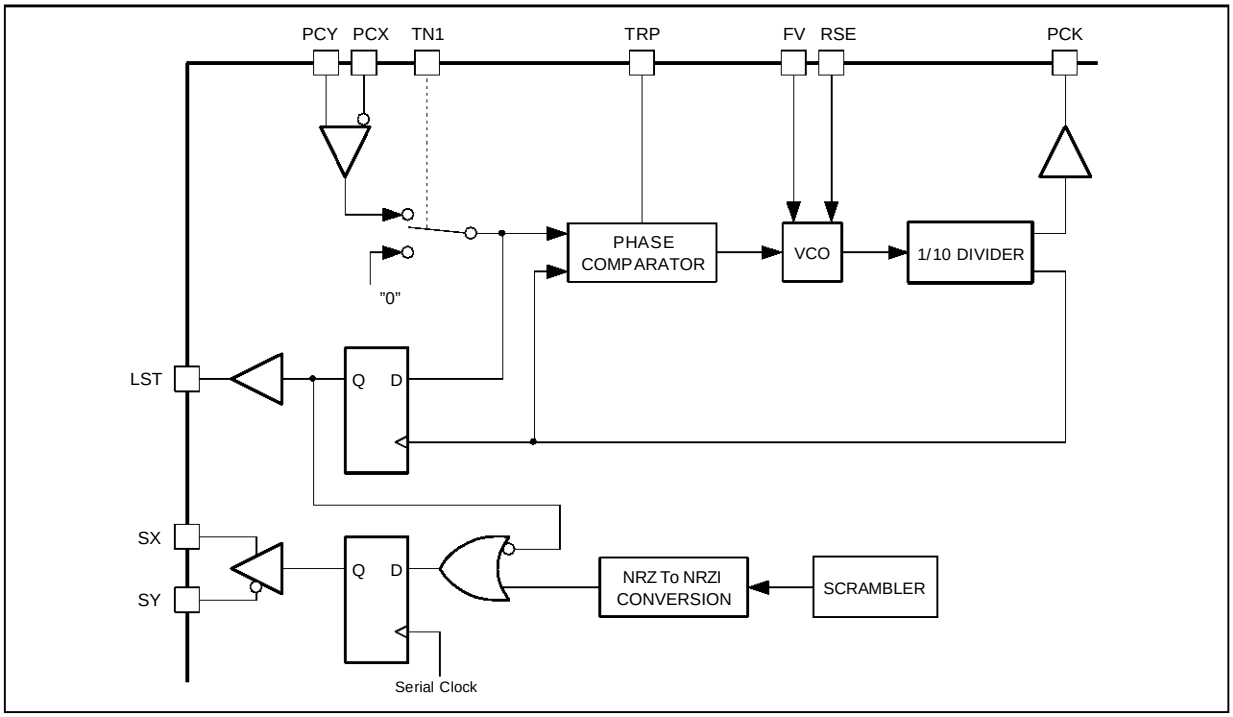
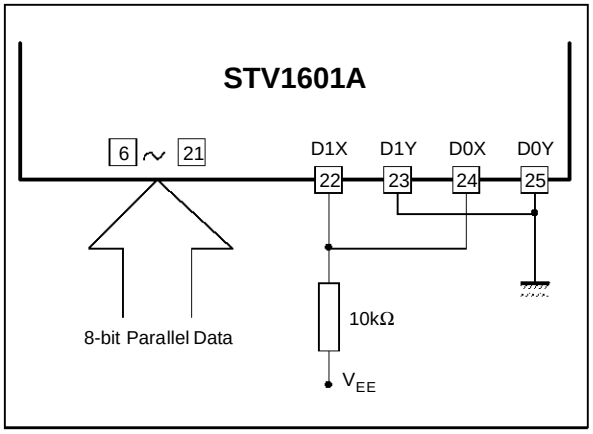
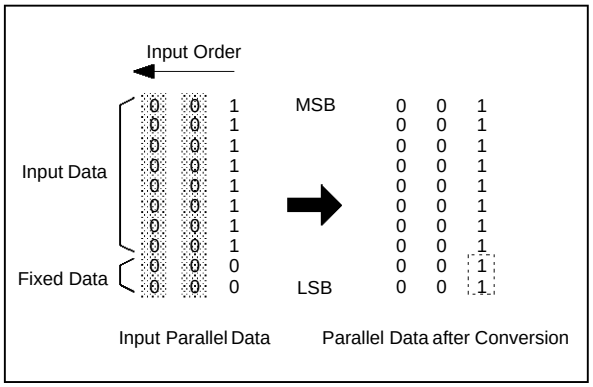


Figure 14 : 8-bit Parallel Input Data (ECL level)



The conversion algorithm detects 2 successive 000H words and sets the two LSBs of the previous word, which is supposed to be FF, according to the standard.

Figure 10 : Conversion from 8-bit TRS to 10-bit TRS



Conversion in the case of more than three successive "000H" words.

If more than 3 consecutive words of 000 in D1 standard, or 4 consecutive words of 000 in D2 standard occur at the parallel input (illegal according to the standard), thus no proper operation is possible.

5. Scrambling and NRZ to NRZI conversion

Figures 16 and 17 show the scrambling circuit, the scrambling polynomial is as follows : $x^9 + x^4 + 1$.

Figure 16 : ($x^9 + x^4 + 1$) Basic Scrambling Circuit

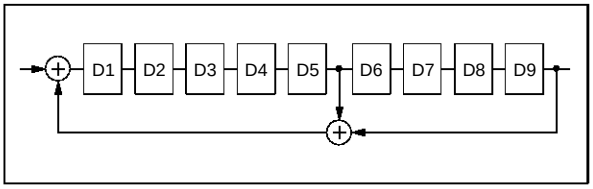
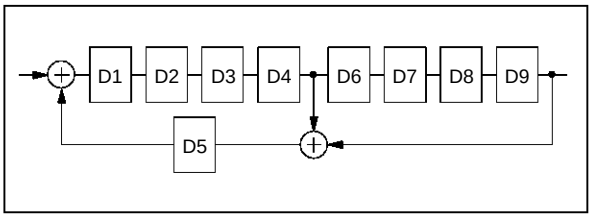


Figure 17 : ($x^9 + x^4 + 1$) Basic Scrambling Circuit



To eliminate signal polarity of scrambled data, conversion from NRZ to NRZI is performed (Figures 18 and 19).

Therefore, the polarity for output distribution or receiving is not needed. This allows easy system design. The NRZ to NRZI polynominal is x + 1.

VCO temperature compensation and oscillation frequency adjustment

VCO oscillation frequency depends on the temperature as shown in Figures 22 and 23 "Representative characteristics examples". Within the normal range of operation, frequency increases with temperature. FV voltage remains almost constant regardless of temperature. Figure 20 shows an example of a temperature compensation circuit using a diode (transistor with C-B diode short-circuited) and a resistor connected between FV and V_{EE}. Examples of representative characteristics for various temperatures are shown in Figures 22 and 23 concerning oscillation frequency and PLL pull-in range (signal frequency 270, 177 and 143MHz).

VCO free running frequency adjustment

VCO free running frequency adjustment is performed at room temperature.

If TN1 is set High, VCO free runs. Wait for 5 to 10 minutes after turning power supply ON (warm up time). While monitoring PCK output (Pin 36) adjust the signal frequency (within ± 1%) with the variable resistor connected between FV and V_{EE}.

Figure 19 : Relation between NRZ and NRZI Signals

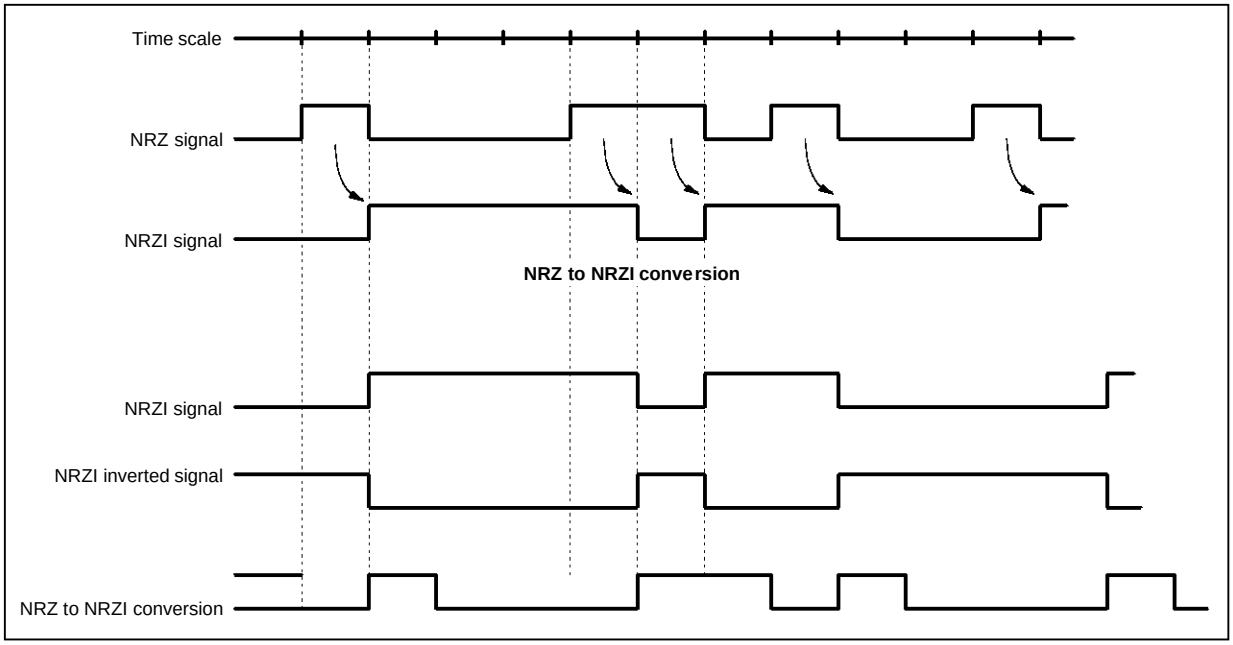
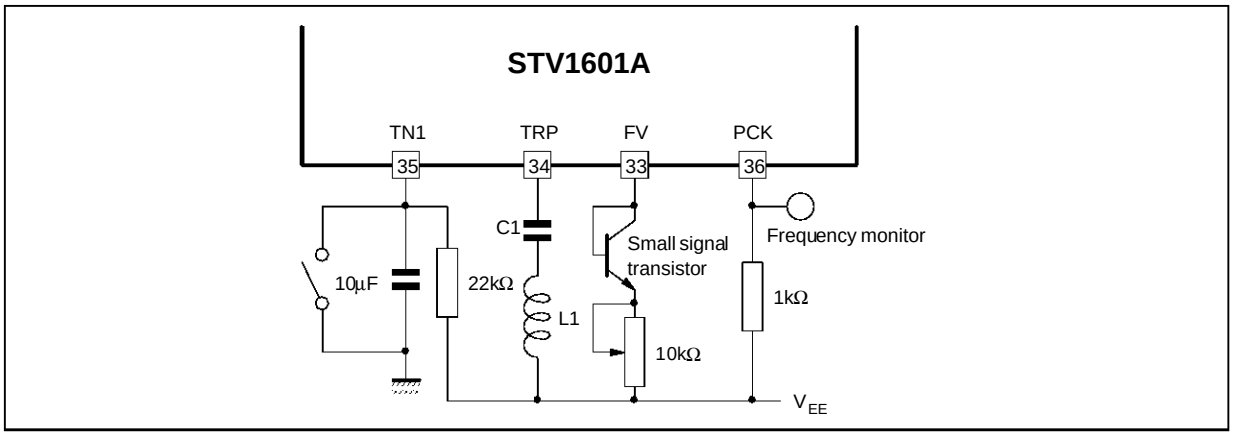


Figure 20 : VCO Temperature Compensation and Free Running Adjustment



Jitter trap

Since the internally generated serial clock is locked to the incoming parallel clock, there exists periodic jitter components which are generated from the phase comparison process of the PLL.

A serial resonant circuit (trap) connected between TRP (Pin 34) and V_{EE} tuned at the parallel clock frequency reduces effectively the fundamental component of the jitter well below the specification (±0.25ns).

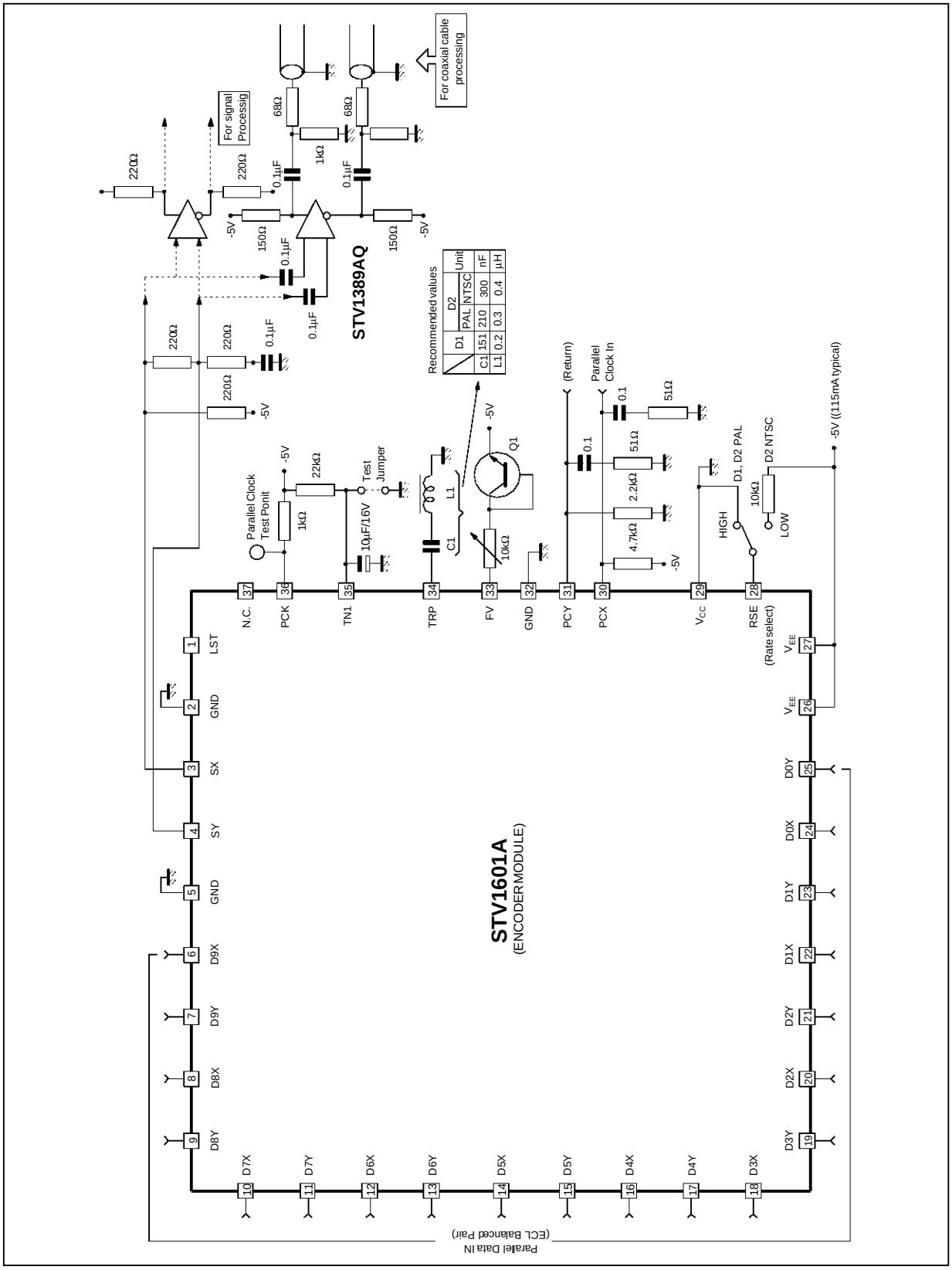
Recommended values of C1 and L1 are given in the following table.

RECOMMENDED VALUES OF THE TRAP CIRCUIT

COMPONENT	STANDARD		
	D1	D2	
		PAL	NTSC
C1 (pF)	150	240	300
L1 (µH)	0.2	0.3	0.4

An important remark in a practical implementation is that TRP node is an input of a very sensitive voltage-frequency converter (VCO) which can be easily disturbed by any pick-up noise.
Hence, the trap circuit should be carefully located and be kept as short as possible from the Pin 34 in order to avoid noise problems.

Figure 21 : Application Circuit Example



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EXAMPLE OF REPRESENTATIVE CHARACTERISTICS

Figure 22 : VCO Oscillation Frequency versus FV Pin Voltage

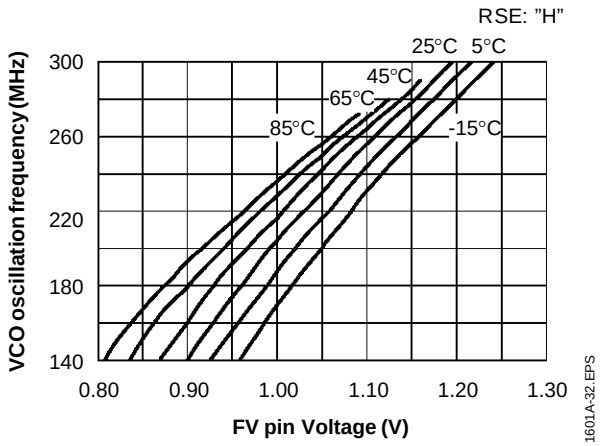


Figure 23 : VCO Oscillation Frequency versus FV Pin Voltage

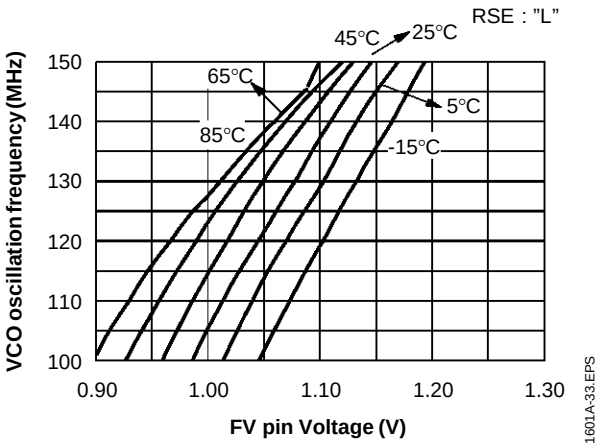


Figure 24 : Pull in Range and Free Run Frequency (270Mb/s)

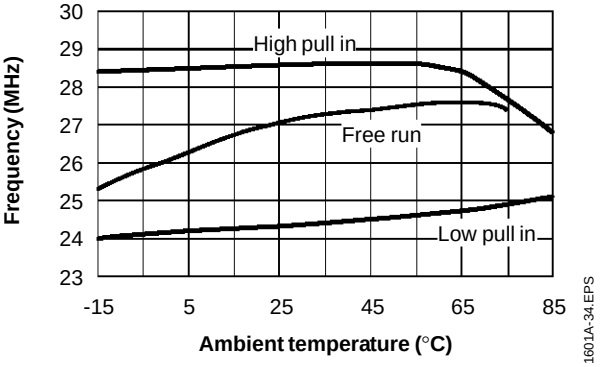


Figure 25 : Pull in Range and Free Run Frequency (177Mb/s)

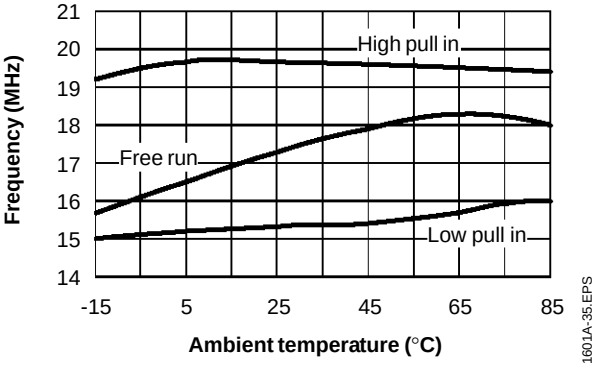
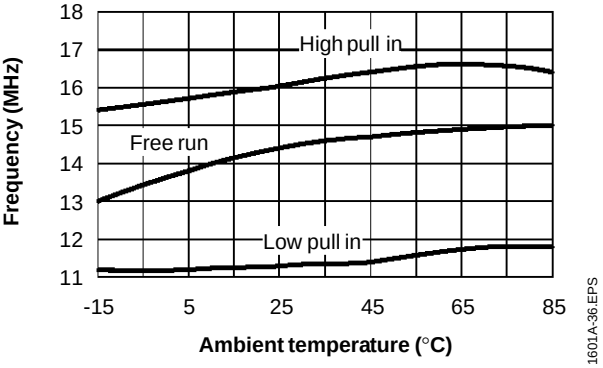
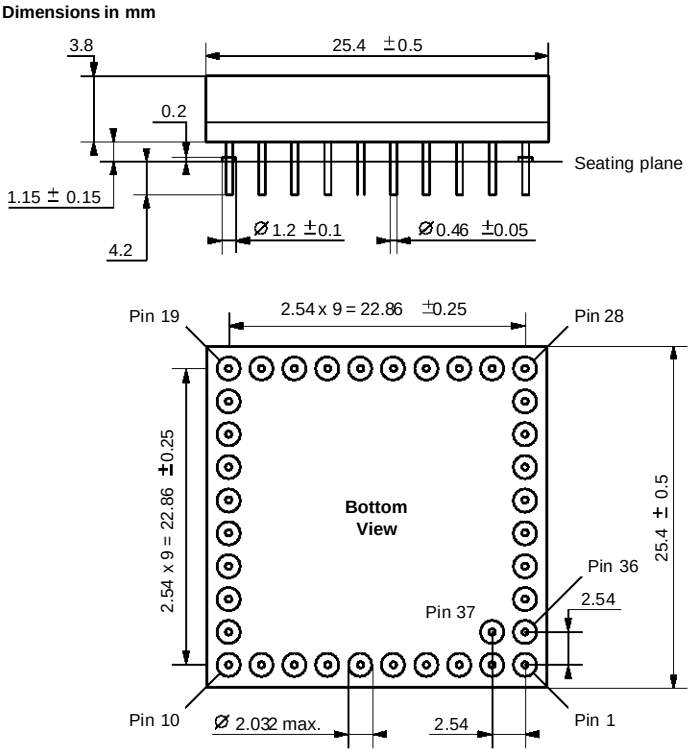


Figure 26 : Pull in Range and Free Run Frequency (143Mb/s)



PACKAGE MECHANICAL DATA

37 PINS - CERAMIC PGA



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